REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add six new device types for vendor CAGE number 65786. Add vendor CAGE number 1FN41 as a source of supply for devices 01KX, 02KX, 03KX, and 04KX. Change to vendor similar part number for vendor CAGE number 1FN41. Change to margin test method A for vendor CAGE 66579. Remove 4.5.1, 4.5.2, 4.5.3, figures 5 and 6, and table III from drawing. Change to parameters t_{CS} and t_{DF} in table I. Change to figures 2 and 3. Editorial changes throughout.	93-01-21	M. A. Frye

REV																			
SHEET																			
REV																			
SHEET																			

REV STATUS OF SHEET															
REV	B	B	B	B	B	B	B	B	B	B	B			
SHEET	1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
James E. Jamison

CHECKED BY
M. A. Frye

APPROVED BY
M. A. Frye

DRAWING APPROVAL DATE
1988-June-21

REV A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, MEMORY, CMOS
8K X 8 UV EPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	5962-87515

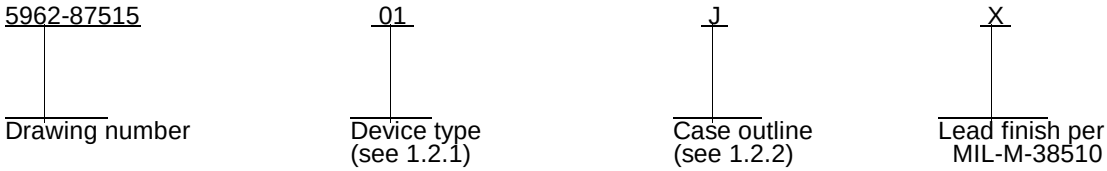
SHEET 1 OF 11

DESC FORM 193
JUL 91

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		8K x 8 UV EPROM	45 ns
02		8K x 8 UV EPROM	55 ns
03		8K x 8 UV EPROM	70 ns
04		8K x 8 UV EPROM	90 ns
05		8K x 8 UV EPROM	45 ns
06		8K x 8 UV EPROM	55 ns
07		8K x 8 UV EPROM	35 ns
08		8K x 8 UV EPROM	35 ns
09		8K x 8 UV EPROM	45 ns
10		8K x 8 UV EPROM	55 ns
11		8K x 8 UV EPROM	25 ns
12		8K x 8 UV EPROM	25 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 OR CDIP2-T24	24	Dual-in-line 2/
K	GDFP2-F24 OR CDFP3-F24	24	Flat pack 2/
L	GDIP3-T24 OR CDIP4-T24	24	Dual-in-line 2/
3	CQCC1-N28	28	Square leadless chip carrier 2/

1.2.3 Lead finish. The lead finish shall be as specified in MIL-M-38510. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Storage temperature	-65°C to +150°C
Voltages on any pin with respect to ground	-0.5 V dc to +7.0 V dc
V_{PP} with respect to ground	-0.5 V dc to +14.0 V dc
Maximum power dissipation (P_D) 3/	1 W
Lead temperature (soldering, 10 seconds	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	MIL-STD-1835
Junction temperature (T_J) 4/	+150°C

1.4 Recommended operating conditions.

Case operating temperature (T_C)	-55°C to +125°C
Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103.
2/ Lid shall be transparent to permit ultraviolet light erasure.
3/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification For.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit case outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMDs).

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3.1 Unprogrammed or erased devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C inspection (see 4.3), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern or equivalent (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total numbers of bits programmed.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^{\circ}C \le T_C \le +125^{\circ}C$ $V_{SS} = 0$ V 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
Input leakage current	I_{LI}	V_{IN} = 5.5 V and GND		1,2,3	All		±10	µA
Output leakage current	I_{LO}	V_{OUT} = 5.5 V and GND		1,2,3	All		±10	µA
Operating supply current (active) 1/	I_{CC1}	$\overline{CS} = V_{IL}$, V_{CC} = 5.5 V D0 to D7 = 0 mA f = max		1,2,3	01-10		120	mA
					11-12		140	
Standby current, TTL inputs	I_{CC2}	$\overline{CS}$ = 2.0 V, V_{CC} = 5.5 V		1,2,3	01-07		40	mA
					12		50	
Standby current, CMOS inputs	I_{CC3}	V_{CC} = 5.5 V, $\overline{CS} = V_{CC}$ -0.3 V		1,2,3	01-07		40	mA
					12		50	
Input low voltage	V_{IL}	V_{CC} = 4.5 V and 5.5 V		1,2,3	All		0.8	V
Input high voltage	V_{IH}	V_{CC} = 4.5 V and 5.5 V		1,2,3	All	2.0		V
Output voltage low	V_{OL}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V	I_{OL} = 16 mA	1,2,3	01-10		0.45	V
			I_{OL} = 6 mA		11,12		0.4	
Output voltage high	V_{OH}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V	I_{OH} = -4 mA	1,2,3	01-10	2.4		V
			I_{OH} = -2 mA		11,12			
Output short circuit current 2/ 3/	I_{OS}	V_O = GND		1,2,3	All		-100	mA
Input capacitance 3/	C_{IN}	f = 1.0 MHz T_C = +25°C See 4.3.1e V_{CC} = 5.5 V	V_{IN} = 0 V	4	All		6	pF
Output capacitance 3/	C_{OUT}		V_{OUT} = 0 V				12	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A sub-groups	Device types	Limits		Unit
					Min	Max	
Address to output delay	t_{ACC}	V_{CC} = 4.5 V See figures 3 and 4	9,10,11	11,12		25	ns
				07,08		35	
				01,05 09		45	
				02,06 10		55	
				03		70	
				04		90	
$\overline{CS}$ to output delay	t_{CS}		9,10,11	11		15	ns
				08		20	
				12		25	
				09		30	
				01,02 10		35	
				07		40	
				05		45	
				03,04, 06		55	
$\overline{CS}$ high to output float 3/ 4/	t_{DF}		9,10,11	11		15	ns
				08,12		25	
				09		30	
				01,02 07,10		35	
				05		45	
				03,04, 06		55	
Address to output hold 3/	t_{OH}		9,10,11	All	0		ns

1/ TTL inputs: $V_{IL} \le 0.8$ V, $V_{IH} \ge 2.0$ V.
2/ Not more than one output should be shorted at a time, and short circuit test (I_{OS}) should not exceed 30 seconds.
3/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
4/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input with the output load in figure 3, circuit B.

Device types	01 - 12	
Case outlines	J,K,L	3
Terminal number	Terminal symbol	
1	A_7	NC
2	A_6	A_7
3	A_5	A_6
4	A_4	A_5
5	A_3	A_4
6	A_2	A_3
7	A_1	A_2
8	A_0	A_1
9	O_0	A_0
10	O_1	NC
11	O_2	O_0
12	GND	O_1
13	O_3	O_2
14	O_4	GND
15	O_5	NC
16	O_6	O_3
17	O_7	O_4
18	A_{12}	O_5
19	A_{11}	O_6
20	$\overline{CS}$	O_7
21	A_{10}	NC
22	A_9	A_{12}
23	A_8	A_{11}
24	V_{CC}	$\overline{CS}$
25	---	A_{10}
26	---	A_9
27	---	A_8
28	---	V_{CC}

FIGURE 1. Terminal connections.

Mode	V_{CC}	$\overline{CS}$/VPP	O_0-O_7
Read	5 V ±10%	V_{IL}	FF H
Output disable	5 V ±10%	V_{IH}	High Z
Program 1/	V_{CC}	V_{PP}	Data i
Verify 1/	V_{CC}	V_{IL}	Programmed byte

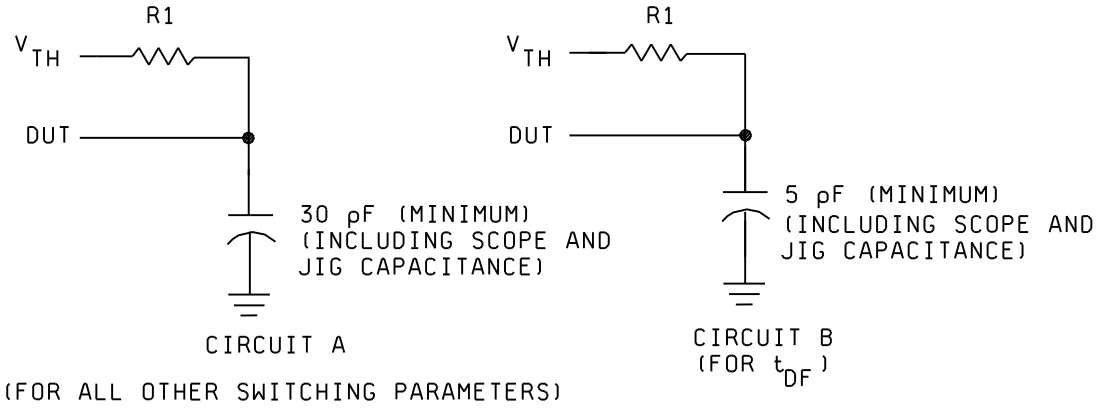
Device types 01-04

Type	Mode	Outputs	A_{12}	A_{11}	$\overline{CS}$	A_{10}	A_9	A_8	V_{CC}	Power
All	Read	D_{OUT}	A_{12}	A_{11}		A_{10}	A_9	A_8	V_{CC}	I_{CC1}
05-07 12	Not selected	High-Z	A_{12}	A_{11}		A_{10}	A_9	A_8	V_{CC}	I_{CC2}, I_{CC3}
08-11	Not selected	High-Z	A_{12}	A_{11}		A_{10}	A_9	A_8	V_{CC}	I_{CC1}
All	Program 1/	D_{IN}	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{ILP}	V_{IHP}	V_{CC}	I_{CC1}
All	Program inhibit 1/	High-Z	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{IHP}	V_{IHP}	V_{CC}	I_{CC1}
All	Program verify 1/	D_{OUT}	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{IHP}	V_{ILP}	V_{CC}	I_{CC1}
All	Blank check 1/	D_{OUT}	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{IHP}	V_{ILP}	V_{CC}	I_{CC1}

1/ See 4.5.

Device types 05-12

FIGURE 2. Truth tables (unprogrammed).



	Device types	
	01-10	11, 12
R1	98 Ω	250 Ω
V_{TH}	2.01 V	1.9 V

FIGURE 3. Output load circuits or equivalent cicuit.

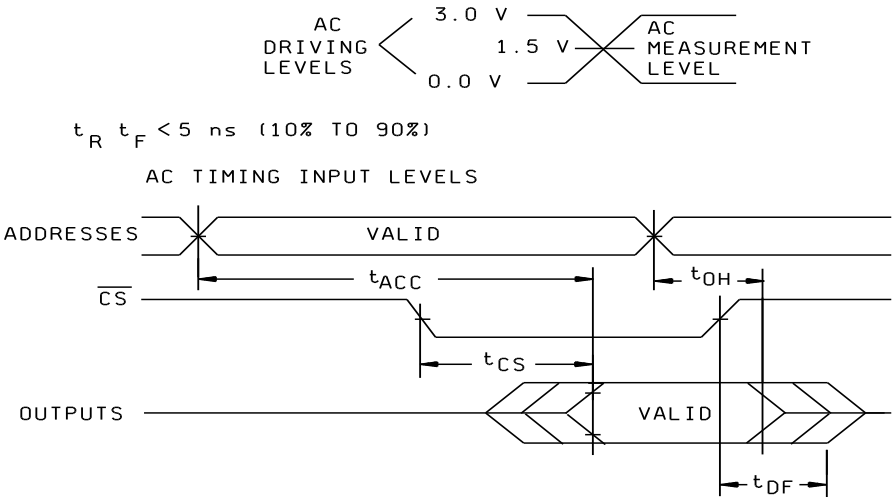


FIGURE 4. AC read timing diagram.

3.6 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.6.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4 herein.

3.6.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 herein.

3.6.3 Verification of erasure of programmed EPROMS. When specified, devices shall be verified as either programmed (see 4.5 herein) to specified program or erased (see 4.4 herein). As a minimum, verification shall consist of performing a funtional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.10 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.7 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A. * Steps 1 through 3 may be performed at wafer level.

(1) At +25°C, program greater than 95 percent of the bit locations, including the slowest programming cell. The remaining bits shall provide a worse case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C or for 48 hours at +150°C or for 8 hours at +200°C or 48 hours at 225°C (unassembled devices only).

(3) At +25°C, perform a margin test using V_m = +5.8 V to loose timing (i.e., t_{ACC} = 1 µs).

(4) Perform dynamic burn-in in accordance with 4.2a.

(5) At +25°C, perform a margin test using V_m = +5.8 V.

(6) Perform electrical test in accordance with 4.2b.

(7) Erase in accordance with 3.6.1. Devices may be submitted to quality conformance inspection.

(8) Verify erasure in accordance with 3.6.3.

Margin test method B.

(1) Program at +25° C greater than 95 percent of the bit locations, including the slowest programming cell. The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at +140° C or for 48 hours at +150° C or for 8 hours at +200° C or for 2 hours at +300° C for unassembled devices only.

(3) Perform margin test using V_m = +5.55 V and V_m = +4.40 V at +25° C using loose timing (i.e., t_{ACC} = 1 µs).

(4) Erase (see 3.6.1).

(4a) Steps 1 through 4 may be performed at the wafer level. The maximum storage temperature shall not exceed +200° C for packaged devices or +300° C for unassembled devices.

(5) Program at +25° C with a 50 percent pattern (checkerboard or equivalent).

(6) Perform margin test using V_m = +5.75 V and V_m = +4.40 V at +25° C with loose timing.

(7) Perform dynamic burn-in in accordance with 4.2a.

(8) Perform margin test using V_m = +5.55 V and V_m = +4.40 V at +25° C using loose timing.

(9) Perform electrical tests (see 4.2b).

(10) Erase (see 3.6.1), except devices submitted for groups A, B, C, and D testing.

(11) Verify erasure (see 3.6.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified except devices being submitted to groups B, C, and D testing.

d. As a minimum, subgroups 7 and 8 shall consist of verifying the EPROM pattern specified.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.7 herein).

(2) T_A = +125° C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. All devices submitted for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 25 Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using a ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum intergrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12,000 $\mu W/cm^2$). Exposure of EPROMS to high intensity UV light for long periods may cause permanent damage.

4.5 Progamming procedure. The progamming procedures shall be as specified by the device manufacturer and shall be made available upon request.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8A,8B, 9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7***, (8A,8B)***,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8A,8B

* PDA applies to subgroup 1 and 7.
** See 4.3.1e.
*** See 4.3.1d.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMDs. All proposed changes to existing SMDs will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone 513-296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.7 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 93-01-21

Approved sources of supply for SMD 5962-87515 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-8751501JX	66579 1FN41	WS57C49C-45DMB AT27HC641R-45DM/883
5962-8751501LX	66579 1FN41	WS57C49C-45TMB AT27HC642R-45DM/883
5962-87515013X	66579 1FN41	WS57C49C-45CMB AT27HC641R-45LM/883
5962-8751501KX	66579 1FN41	WS57C49C-45FMB AT27HC641R-45FM/883
5962-8751502JX	66579 1FN41	WS57C49C-55DMB AT27HC641R-55DM/883
5962-8751502LX	66579 1FN41	WS57C49C-55TMB AT27HC642R-55DM/883
5962-87515023X	66579 1FN41	WS57C49C-55CMB AT27HC642R-55LM/883
5962-8751502KX	66579 1FN41	WS57C49C-55FMB AT27HC642R-55FM/883
5962-8751503JX	66579 1FN41	WS57C49C-70DMB AT27HC641R-70DM/883
5962-8751503LX	66579 1FN41	WS57C49C-70TMB AT27HC642R-70DM/883
5962-87515033X	66579 1FN41	WS57C49C-70CMB AT27HC641R-70LM/883
5962-8751503KX	66579 1FN41	WS57C49C-70FMB AT27HC641R-70FM/883

See footnote at end of table.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-8751504JX	66579 1FN41	WS57C49C-90DMB AT27HC641R-90DM/883
5962-8751504LX	66579 1FN41	WS57C49C-90TMB AT27HC642R-90DM/883
5962-87515043X	66579 1FN41	WS57C49C-90CMB AT27HC641R-90LM/883
5962-8751504KX	66579 1FN41	WS57C49C-90FMB AT27HC641R-90FM/883
5962-8751505LX	65786	CY7C261-45WMB
5962-87515053X	65786	CY7C261-45QMB
5962-8751505KX	65786	CY7C261-45TMB
5962-8751506LX	65786	CY7C261-55WMB
5962-87515063X	65786	CY7C261-55QMB
5962-8751506KX	65786	CY7C261-55TMB
5962-8751507LX	65786 66579	CY7C261-35WMB WS57C49C-35TMB
5962-87515073X	65786 66579	CY7C261-35QMB WS57C49C-35CMB
5962-8751507KX	65786 66579	CY7C261-35TMB WS57C49C-35FMB
5962-8751508JX	65786	CY7C264-35WMB
5962-8751508LX	65786 66579	CY7C263-35WMB WS57C49C-35TMB
5962-87515083X	65786 66579	CY7C263-35QMB WS57C49C-35CMB
5962-8751508KX	65786 66579	CY7C263-35TMB WS57C49C-35FMB
5962-8751509JX	65786	CY7C264-45WMB
5962-8751509LX	65786	CY7C263-45WMB
5962-87515093X	65786	CY7C263-45QMB
5962-8751509KX	65786	CY7C263-45TMB
5962-8751510JX	65786	CY7C264-55WMB
5962-8751510LX	65786	CY7C263-55WMB

See footnote at end of table.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-87515103X	65786	CY7C263-55QMB
5962-8751510KX	65786	CY7C263-55TMB
5962-8751511JX	65786	CY7C264-25WMB
5962-8751511LX	65786	CY7C263-25WMB
5962-87515113X	65786	CY7C263-25QMB
5962-8751511KX	65786	CY7C263-25TMB
5962-8751512LX	65786	CY7C261-25WMB
5962-87515123X	65786	CY7C261-25QMB
5962-8751512KX	65786	CY7C261-25TMB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address	Margin test method
66579	WaferScale Intergration Inc. 47280 Kato Road Fremont, CA 94538	A
1FN41	ATMEL Corporation 2125 O'Nel Drive San Jose, CA 95131	A
65786	Cypress Semiconductor Corporation 3901 North First Street San Jose, CA 95134	B